AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-47 (canceled)

48. (New) A voltage clamping circuit comprising:

an input terminal to which an input voltage is supplied;

a MOSFET which has either one of source/drain routes thereof connected to the input terminal and has a predetermined voltage supplied to a gate thereof; and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit, wherein

the voltage clamping circuit obtains an output voltage from another source/drain route of the MOSFET.

49. (New) A voltage clamping circuit according to claim 48, wherein

a capacitor is provided in parallel to the current source.

50. (New) A voltage clamping circuit according to claim 49, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

51. (New) A voltage clamping circuit according to claim 50, wherein

the output voltage is supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage.

52. (New) A voltage clamping circuit according to claim 48, wherein

the voltage clamping circuit is mounted on a semiconductor integrated circuit device, and

the input terminal is an external terminal of the semiconductor integrated circuit device, and an electrostatic breakdown preventing circuit is provided thereto.

53. (New) A voltage clamping circuit according to claim 51, wherein

an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on a next stage, and

an output signal of the second CMOS inverter circuit is fed back to a gate of the MOSFET which is provided between an input terminal of the second CMOS inverter circuit and a ground potential of the circuit thus allowing the first CMOS inverter circuit to possess a hysteresis transmission characteristic.

54. (New) A voltage clamping circuit according to claim 52, wherein

the MOSFET is of an N-channel type, and

the input voltage assumes a positive voltages.

55. (New) A voltage clamping circuit according to claim 48, wherein

the current source allows a DC current component to flow therethrough.

56. (New) A voltage clamping circuit according to claim 55, wherein

a capacitor is provided in parallel to the current source.

57. (New) A voltage clamping circuit according to claim 56, wherein

the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage, and the predetermined voltage is the power source voltage, and

the input circuit includes a capacitive component in parallel to the capacitor.

58. (New) A voltage clamping circuit according to claim 48, wherein

a substrate of the MOSFET is connected to another source/drain route of the MOSFET.

59. (New) A voltage level shifting circuit comprising:

a MOSFET which has either one of source/drain routes thereof connected to an input node to which an input voltage is supplied and has a predetermined voltage supplied to a gate thereof;

a current source which is provided between another source/drain route of the MOSFET and a ground potential of

the circuit and allows a DC current component to flow therethrough, wherein

the voltage level shifting circuit obtains an output voltage from another source/drain route of the MOSFET.

60. (New) A voltage level shifting circuit according to claim 59, wherein

a capacitor is provided in parallel to the current source.

61. (New) A voltage level shifting circuit according to claim 60, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

62. (New) A voltage level shifting circuit according to claim 61, wherein

the output voltage is supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage, and

the predetermined voltage is the power source voltage.

63. (New) A voltage level shifting circuit according to claim 59, wherein

the voltage level shifting circuit is mounted on one semiconductor substrate.

64. (New) A voltage level shifting circuit according to claim 63, wherein

the voltage level shifting circuit is mounted on a semiconductor integrated circuit device, and

the input node is an external terminal of the semiconductor integrated circuit device, and an electrostatic breakdown preventing circuit is provided thereto.

65. (New) A voltage level shifting circuit according to claim 61, wherein

an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on a next stage, and

an output signal of the second CMOS inverter circuit is fed back to a gate of the MOSFET which is provided between an input terminal of the second CMOS inverter circuit and a ground potential of the circuit thus allowing the first CMOS

inverter circuit to possess a hysteresis transmission characteristic.

66. (New) A voltage level shifting circuit according to claim 62, wherein

the MOSFET and the depression MOSFET are of an N-channel type, and

the input voltage and the power source voltage assume a positive voltages.

67. A voltage level shifting circuit according to claim 60, wherein

the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage,

the predetermined voltage is the power source voltage, and

the input circuit includes a capacitive component in parallel to the capacitor.

68. (New) A voltage level shifting circuit according to claim 59, wherein

a substrate of the MOSFET is connected to another source/drain route of the MOSFET.

69. (New) A switching power source device comprising:

an inductor;

a first capacitor which is provided in series with the inductor and forms an output voltage;

a first switching element which controls a current which is made to flow in the inductor by performing a switching control of an input voltage;

a second switching element which performs a switching operation which possesses time in which the second switching element assumes an ON state when the first switching element assumes an OFF state thus controlling the current;

a first driving circuit which is operated by a first voltage corresponding to an input voltage thus driving the first switching element;

a second driving circuit which is operated by a second voltage thus driving the second switching element;

a control circuit which forms a PWM signal so that the output voltage which is obtained from the first capacitor becomes a predetermined voltage; and

a control logic circuit which is operated by the input voltage or a third voltage which is lower than the second voltage, and forms a driving signal for the first driving

circuit and the second driving circuit by receiving the PWM signal, wherein

the control logic circuit includes a first voltage clamping circuit which performs voltage clamping of a driving signal for the first switching element in response to the third voltage and feedbacks the driving signal for the first switching element to an input of the second driving circuit, and a second voltage clamping circuit which performs voltage clamping of a driving signal for the second switching element in response to the third voltage and feedbacks the driving signal for the second switching element to an input of the first driving circuit, and performs a switching control to prevent the first and second switching elements from simultaneously assuming an ON state, and

the first and second voltage clamping circuits respectively include

an input node,

a MOSFET which has either one of source/drain routes connected to the input node and the third voltage supplied to a gate thereof; and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit, wherein

the voltage clamping circuit obtains a feedback signal which is generated by performing the voltage clamping of the signal from the input node from another source/drain route of the MOSFET.

70. (New) A switching power source device according to claim 69, wherein

the switching power source device includes a third voltage clamping circuit, and

the third voltage clamping circuit is constituted of

an input node to which an input signal for controlling an active/reactive (ON/OFF) state of the switching power source device,

a MOSFET which has either one of the source/drain routes thereof connected to the input node and has the third voltage supplied to a gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and the ground potential of the circuit, wherein

the voltage clamping circuit obtains control signal which is generated by performing the voltage clamping of the input signal from another source/drain route of the MOSFET.

71. (New) A switching power source device according to claim 69, wherein

a second capacitor is provided in parallel to the current source.

72. (New) A switching power source device according to claim 71, wherein

the second capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is formed of a depression type MOSFET which connects a gate and a source thereof to each other.

73. (New) A switching power source device according to claim 69, wherein

the current source allows a DC current component to flow therethrough.

74. (New) A switching power source device according to claim 73, wherein

a second capacitor is provided in parallel to the current source.

75. (New) A switching power source device according to claim 74, wherein

the feedback signal is supplied to an input part of the control logic circuit which is operated with the third voltage smaller than the driving signal.

76. (New) A semiconductor integrated circuit device comprising:

a first switching element which controls a current for forming an output voltage by dropping an input voltage;

a terminal which allows the current to pass therethrough;

a second switching element which performs a switching operation which possess time in which the second switching element assumes an ON state when the first switching element assumes an OFF state thus controlling the current;

a first driving circuit which is operated by a first voltage corresponding to an input voltage thus driving the first switching element;

a second driving circuit which is operated by a second voltage thus driving the second switching element; and

a control logic circuit which is operated by the input voltage or a third voltage which is equal to or less than

the second voltage, and forms a driving signal for the first driving circuit and the second driving circuit by receiving control signals for the first switching element and the second switching element, wherein

the control logic circuit includes a first voltage level shifting circuit which shifts a voltage level of a driving signal for the first switching element in response to the third voltage and feedbacks the driving signal of the first switching element to an input of the second driving circuit, and a second voltage level shifting circuit which shifts a voltage level of a driving signal for the second switching element in response to the third voltage and feedbacks the driving signal for the second switching element to an input of the first driving circuit, and performs a switching control to prevent the first and second switching elements from simultaneously assuming an ON state, and

the first switching element, the terminal, the second switching element, the first driving circuit, the second driving circuit and the control logic circuit are sealed in one package.

77. (New) A semiconductor integrated circuit device according to claim 76, wherein

the control signal is a PWM signal, and

the first and second voltage level shifting circuits respectively include

an input node to which the driving signal is supplied,

a MOSFET which has either one of source/drain routes thereof connected to the input node and has the third voltage supplied to the gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough, wherein

the semiconductor integrated circuit device obtains a feedback signal which is generated by shifting a voltage level of the driving signal from another source/drain route of the MOSFET.

78. (New) A semiconductor integrated circuit device according to claim 76, wherein

the control signal is a PWM signal,

the semiconductor integrated circuit device further includes a third voltage level shifting circuit,

the third voltage level shifting circuit is sealed in one package, and

the third voltage level shifting circuit includes

an input terminal to which an input signal for controlling an active/reactive (ON/OFF) state of the semiconductor integrated circuit device is supplied,

a MOSFET which has either one of the source/drain routes thereof connected to the input terminal and has the third voltage supplied to the gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of a circuit and allows a DC current component to flow therethrough, and

the third voltage level shifting circuit obtains a control signal which is formed by shifting a voltage level of the input signal from another source/drain route of the MOSFET.

79. (New) A semiconductor integrated circuit device according to claim 77, wherein

a capacitor is provided in parallel to the current source.

80. (New) A semiconductor integrated circuit device according to claim 79, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

81. (New) A semiconductor integrated circuit device according to claim 77, wherein

the feedback signal is transmitted to an input part of the control logic circuit which is operated with the third voltage smaller than the driving signal.

82. (New) A semiconductor integrated circuit device according to claim 76, wherein

the current is a current which is made to flow in the inductor from a generating part of the input voltage to form the output voltage by the inductor and the capacity which is provided in series with the inductor.

83. (New) A voltage level shifting circuit comprising:

an input terminal to which an input voltage is supplied;

a MOSFET which has either one of source/drain routes thereof connected to the input terminal and has a predetermined voltage supplied to a gate thereof; and

a part which is provided between another source/drain route of the MOSFET and a ground potential of the circuit, wherein

the voltage level shifting circuit obtains an output voltage from another source/drain route of the MOSFET, and

when the input voltage is equal to or more than a voltage corresponding to the predetermined voltage, the output voltage corresponding to the predetermined voltage is outputted from another source/drain route, and

the part is configured such that a current which brings a voltage of another source/drain route close to the ground potential is allowed to flow in the part when a voltage larger than the ground potential is applied to another source/drain route.

84. (New) A voltage level shifting circuit according to claim 83, wherein

when the input voltage is less than a voltage corresponding to the predetermined potential, the output voltage corresponding to the input voltage is outputted from another source/drain route.

85. (New) A voltage level shifting circuit according to claim 83, wherein

a current which brings a voltage of another source/drain route close to the ground potential is a fine current which is not considered as a defect of the voltage level shifting circuit.

86. (New) A voltage level shifting circuit according to claim 83, wherein

a capacitor is provided in parallel to the part.

87. (New) A voltage level shifting circuit according to claim 83, wherein

the part is a depression type MOSFET which connects a gate and a source thereof to each other.

88. (New) A voltage level shifting circuit according to claim 83, wherein

the part is a resistance element formed of poly-silicon.

89. (New) A voltage level shifting circuit according to claim 86, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET.

90. (New) A semiconductor integrated circuit device according to claim 76, wherein

the first switching element is formed on a first semiconductor substrate,

the second switching element is formed on a second semiconductor substrate, and

the first and second semiconductor substrates are sealed in one package.

91. (New) A semiconductor integrated circuit device according to claim 90, wherein

the first driving circuit, the second driving circuit and the control logic circuit are formed on the third semiconductor substrate, and

the third semiconductor substrate is sealed in one package.

92. (New) A semiconductor integrated circuit device according to claim 76, wherein

the first switching element, the second switching element, the first driving circuit, the second driving circuit and the control logic circuit are formed on one semiconductor substrate, and one semiconductor substrate is sealed in one package.

93. (New) A semiconductor integrated circuit device according to claim 76, wherein

the semiconductor integrated circuit device includes

a first control terminal to which an input signal for controlling an active/reactive state of the semiconductor integrated circuit device is supplied,

a second control terminal which receives the PWM signal,

a power source terminal which supplies the second voltage, and

the second voltage is allowed to be set arbitrarily within a predetermined range by supplying a power source to the power source terminal from outside.

94. (New) A semiconductor integrated circuit device according to claim 93, wherein the semiconductor integrated circuit device includes a detection circuit for detecting

the input voltage and controls the control logic circuit in accordance with a detection result.